IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Previously Presented) A processor comprising:

a first register configured to store a first target address;

a second register configured to store a second target address;

a third register; and

an execution core coupled to the first register, the second register, and the third register, wherein the execution core is configured, responsive to a first instruction, to: (i) select the first target address from the first register as a next program counter address if a first operating mode is active in the processor, and (ii) select the second target address from the second register as the next program counter address if a second operating mode is active in the processor; and wherein the execution core is configured to store a first address in the third register responsive to the first instruction, wherein the first address is an address of a second instruction following the first instruction.

2. (Previously Presented) The processor as recited in claim 1 further comprising a fourth register coupled to the execution core, a code segment register coupled to the execution core, and a stack segment register coupled to the execution core, wherein the execution core is configured, responsive to the first instruction, to: (i) read a first segment selector from the fourth register, (ii) store the first segment selector in the code segment register, and (iii) generate a second segment selector from the first segment selector and store the second segment selector in the stack segment register.

3. (Previously Presented) The processor as recited in claim 2 wherein the fourth register

is further configured to store a third target address, and wherein the execution core is configured, responsive to the first instruction, to select the third target address as the next program counter address if a third operating mode is active in the processor.

4. (Original) The processor as recited in claim 1 wherein the first operating mode includes a default address size greater than 32 bits.

5. (Original) The processor as recited in claim 1 further comprising a segment register configured to store a segment selector and at least a first operating mode indication and a second operating mode indication from a segment descriptor indicated by the segment selector, and still further comprising a configuration register storing an indication, wherein the processor is configured to generate an operating mode in response to the first operating mode indication, the second operating mode indication, and the indication in the configuration register.

6. (Cancelled)

7. (Previously Presented) The processor as recited in claim 1 wherein the execution core, responsive to a third instruction, is configured to branch to the first address, the processor further comprising a fourth register configured to store a first segment selector, and wherein the execution core is configured, responsive to the third instruction, to generate a second segment selector from the first segment selector responsive to an operand size of the third instruction.

8. (Original) The processor as recited in claim 7 wherein the operand size of the third instruction is responsive to a prefix byte of the third instruction.

9. (Original) The processor as recited in claim 7 wherein the second segment selector is equal to the first segment selector responsive to the operand size being 32 bit, and wherein the second segment selector is equal to the first segment selector incremented by a constant responsive to the operand size being 64 bit.

10. (Previously Presented) The processor as recited in claim 9 wherein the execution core is configured to modify a first operating mode indication and a second operating mode indication stored in a code segment register responsive to the operand size of the third instruction.

11. (Previously Presented) An apparatus comprising:

a first storage location corresponding to a first register, the first storage location storing a first target address;

a second storage location corresponding to a second register, the second storage location storing a second target address;

a third storage location; and

a processor coupled to the first storage location, the second storage location, and the third storage location, wherein the processor is configured, responsive to a first instruction, to: (i) select the first target address from the first storage location as a next program counter address if a first operating mode is active, and (ii) select the second target address from the second storage location as the next program counter address if a second operating mode is active, and wherein the processor is configured to store a first address in the third storage location responsive to the first instruction, wherein the first address is an address of a second instruction following the first instruction.

12. (Previously Presented) The apparatus as recited in claim 11 further comprising a fourth storage location corresponding to a fourth register, a fifth storage location corresponding to a code segment register, and a sixth storage location corresponding to a stack segment register, wherein the processor is configured, responsive to the first

instruction, to: (i) read a first segment selector from the fourth storage location, (ii) store the first segment selector in the fifth storage location, and (iii) generate a second segment selector from the first segment selector and store the second segment selector in the sixth storage location.

13. (Previously Presented) The apparatus as recited in claim 12 wherein the fourth storage location further stores a third target address, and wherein the processor is configured, responsive to the first instruction, to select the third target address as the next program counter address if a third operating mode is active.

14. (Original) The apparatus as recited in claim 11 wherein the first operating mode includes a default address size greater than 32 bits.

15. (Previously Presented) The apparatus as recited in claim 11 further comprising a seventh storage location corresponding to a segment register, the seventh storage location storing a segment selector and at least a first operating mode indication and a second operating mode indication from a segment descriptor indicated by the segment selector, the apparatus still further comprising an eighth storage location storing an indication, wherein the processor is configured to generate an operating mode in response to the first operating mode indication, the second operating mode indication, and the indication in the eighth storage location.

16. (Cancelled)

17. (Previously Presented) The apparatus as recited in claim 11 wherein the processor, responsive to a third instruction, is configured to branch to the first address, the apparatus further comprising a fourth storage location configured to store a first segment selector, and wherein the processor is configured, responsive to the third instruction, to generate a second segment selector from the first segment selector responsive to an operand size of the third instruction.

18. (Original) The apparatus as recited in claim 17 wherein the operand size of the third instruction is responsive to a prefix byte of the third instruction.

19. (Original) The apparatus as recited in claim 17 wherein the second segment selector is equal to the first segment selector responsive to the operand size being 32 bit, and wherein the second segment selector is equal to the first segment selector incremented by a constant responsive to the operand size being 64 bit.

20. (Previously Presented) The apparatus as recited in claim 19 wherein the execution core is configured to modify a first operating mode indication and a second operating mode indication stored in a fifth storage location responsive to the operand size of the third instruction.

21. (Previously Presented) A method comprising:

selecting a first target address from a first register as a next program counter address responsive to a first operating mode during execution of a first instruction;

selecting a second target address from a second register as the next program counter address responsive to a second operating mode during execution of the first instruction; and

storing a first address in a third register responsive to executing the first instruction, wherein the first address is an address of a second instruction following the first instruction.

22. (Previously Presented) The method as recited in claim 21 further comprising, responsive to executing the first instruction:

reading a first segment selector from a fourth register;

storing the first segment selector in a code segment register;

generating a second segment selector from the first segment selector; and

storing the second segment selector in a stack segment register.

23. (Previously Presented) The method as recited in claim 22 wherein the fourth register is further configured to store a third target address, the method further comprising, responsive to the first instruction, selecting the third target address as the next program counter address during execution of the first instruction responsive to a third operating mode.

24. (Previously Presented) The method as recited in claim 21 wherein the first operating mode includes a default address size greater than 32 bits.

25. (Original) The method as recited in claim 21 further comprising generating an operating mode in response to a first operating mode indication, a second operating mode indication, and an indication in a configuration register, wherein a segment register is configured to store a segment selector and at least the first operating mode indication and the second operating mode indication from a segment descriptor indicated by the segment selector.

26. (Cancelled)

27. (Previously Presented) The method as recited in claim 21 further comprising, responsive to a third instruction:

branching to the first address; and

generating a second segment selector from a first segment selector stored in a

fourth register responsive to an operand size of the third instruction.

28. (Original) The method as recited in claim 27 wherein the operand size of the third instruction is responsive to a prefix byte of the third instruction.

29. (Original) The method as recited in claim 27 wherein the generating comprises:

generating the second segment selector equal to the first segment selector responsive to the operand size being 32 bit; and

generating the second segment selector equal to the first segment selector incremented by a constant responsive to the operand size being 64 bit.

30. (Previously Presented) The method as recited in claim 29 further comprising modifying a first operating mode indication and a second operating mode indication stored in a code segment register responsive to the operand size of the third instruction.

31. (Currently Amended) A tangible computer readable medium storing a plurality of instructions which, when executed responsive to an occurrence of a first instruction in a code sequence:

select a first target address from a first storage location corresponding to a first register as a next program counter address if a first operating mode is active;

select a second target address from a second storage location corresponding to a second register as the next program counter address if a second operating mode is active; and

store a first address in a third storage location responsive to the first instruction, wherein the first address is an address of a second instruction following

the first instruction.

32. (Previously Presented) The computer readable medium as recited in claim 31 wherein the plurality of instructions emulate the first instruction.

33. (Previously Presented) The computer readable medium as recited in claim 31 wherein the plurality of instructions are executed in place of the first instruction.

34. (Currently Amended) The computer readable medium as recited in claim 31 wherein the plurality of instructions, when executed responsive to the occurrence of the first instruction:

read a first segment selector from a fourth storage location corresponding to a fourth register;

store the first segment selector in a fifth storage location corresponding to a code segment register; and

generate a second segment selector from the first segment selector and store the second segment selector in a sixth storage location corresponding to a stack segment register.

35. (Currently Amended) The computer readable medium as recited in claim 34 wherein the fourth storage location further stores a third target address, and wherein the plurality of instructions, when executed responsive to the occurrence of the first instruction, select the third target address as the next program counter address if a third operating mode is active.

36. (Previously Presented) The computer readable medium as recited in claim 31 wherein the first operating mode includes a default address size greater than 32 bits.

37. (Currently Amended) The computer readable medium as recited in claim 31 wherein a seventh storage location corresponds to a segment register, the seventh storage location storing a segment selector and at least a first operating mode indication and a second operating mode indication from a segment descriptor indicated by the segment selector, and an eighth storage location stores an indication, wherein the plurality of instructions, when executed responsive to the occurrence of the first instruction, generate an operating mode in response to the first operating mode indication, the second operating mode indication, and the indication in the eighth storage location.

38. (Currently Amended) The computer readable medium as recited in claim 31 further storing a second plurality of instructions executed responsive to an occurrence of a third instruction, wherein the second plurality of instructions, when executed, branch to the first address, and wherein a fourth storage location stores a first segment selector, and wherein the second plurality of instructions, when executed responsive to the occurrence of the third instruction, generate a second segment selector from the first segment selector responsive to an operand size of the third instruction.

39. (Previously Presented) The computer readable medium as recited in claim 38 wherein the operand size of the third instruction is responsive to a prefix byte of the third instruction.

40. (Previously Presented) The computer readable medium as recited in claim 38 wherein the second segment selector is equal to the first segment selector responsive to the operand size being 32 bit, and wherein the second segment selector is equal to the first segment selector incremented by a constant responsive to the operand size being 64 bit.

41. (Currently Amended) The computer readable medium as recited in claim 40 wherein the second plurality of instructions, when executed responsive to the occurrence of the third instruction, modify a first operating mode indication and a second operating mode indication stored in a fifth storage location responsive to the operand size of the third

instruction.

42. (Previously Presented) A computer system comprising the processor as recited in claim 1 and a peripheral device configured to communicate between the computer system and another computer system.

43. (Previously Presented) A processor comprising:

a first register configured to store a first address; and

an execution core coupled to the first register, wherein the execution core is configured to select the first address as a next program counter address responsive to a first instruction, and wherein the first instruction has an associated operand size, and wherein the execution core is configured to establish, responsive to the first instruction, an operating mode in the processor for executing a second instruction stored at the first address, the operating mode selected from a plurality of operating modes responsive to the operand size of the first instruction.

44. (Previously Presented) The processor as recited in claim 43 wherein the operand size is specified via a prefix of the first instruction.

45. (Previously Presented) The processor as recited in claim 43 further comprising a code segment register and a second register configured to store a first segment selector, and wherein the execution core is configured, responsive to the operand size of the first instruction being a first size, to store the first segment selector in the code segment register.

46. (Previously Presented) The processor as recited in claim 45 wherein the execution core is configured, responsive to the operand size of the first instruction being a second

size, to store the first segment selector incremented by a constant in the code segment register.

47. (Previously Presented) A computer system comprising the processor as recited in claim 43 and a peripheral device configured to communicate between the computer system and another computer system.

48. (Previously Presented) An apparatus comprising:

a first storage location corresponding to a first register, the first storage location configured to store a first address; and

a processor coupled to the first storage location, wherein the processor is configured to select the first address as a next program counter address responsive to a first instruction, and wherein the first instruction has an associated operand size, and wherein the processor is configured to establish, responsive to the first instruction, an operating mode in the processor for executing a second instruction stored at the first address, the operating mode selected from a plurality of operating modes responsive to the operand size of the first instruction.

49. (Previously Presented) The apparatus as recited in claim 48 wherein the operand size is specified via a prefix of the first instruction.

50. (Previously Presented) The apparatus as recited in claim 48 further comprising a second storage location corresponding to a code segment register and a third storage location corresponding to a second register, the third storage location configured to store a first segment selector, and wherein the processor is configured, responsive to the operand size of the first instruction being a first size, to store the first segment selector in the second storage location.

51. (Previously Presented) The apparatus as recited in claim 50 wherein the processor is configured, responsive to the operand size of the first instruction being a second size, to store the first segment selector incremented by a constant in the second storage location.

52. (Currently Amended) A tangible computer readable medium storing a plurality of instructions which, when executed responsive to a first instruction having an associated operand size:

select a first address stored in a first storage location corresponding to a first register as a next program counter address; and

establish an operating mode for executing a second instruction stored at the first address, the operating mode selected from a plurality of operating modes responsive to the operand size of the first instruction.

53. (Previously Presented) The computer readable medium as recited in claim 52 wherein the operand size is specified via a prefix of the first instruction.

54. (Previously Presented) The computer readable medium as recited in claim 52 wherein a second storage location corresponds to a code segment register and a third storage location corresponds to a second register, the third storage location configured to store a first segment selector, and wherein the plurality of instructions, when executed responsive to the first instruction, store the first segment selector in the second storage location responsive to the operand size being a first size.

55. (Previously Presented) The computer readable medium as recited in claim 54 wherein the plurality of instructions, when execute responsive to the first instruction, store the first segment selector incremented by a constant in the second storage location responsive to the operand size being a second size.